IN THE CLAIMS:

1. (Currently Amended) An electrical circuit board comprising:

X wiring lines and Y segmented wiring lines, each of the wiring lines being formed of a same conductive metal film and in a same plane on an insulating substrate and the Y segmented wiring lines intersecting ~~with~~ the X wiring ~~lines,~~ lines and being severed ~~by the X wiring lines~~ at the intersections with the X wiring lines, and ~~being distanced~~ spaced apart from the X wiring lines;

wherein top and side surfaces of the X wiring lines are covered with an insulating film; ~~and~~

segments of each of the Y segmented wiring lines are electrically connected together by a Y segmented wiring line-connecting electrode formed on the insulating ~~film.~~film, the Y segments being spaced apart by the X wiring lines and the covering insulating film; wherein

the insulating film covering the side surfaces of the X wiring lines is an insulating metal oxide film formed by oxidizing the side surfaces of the X wiring lines.

2. (Cancelled)

3. (Currently Amended) The electrical circuit board according to claim ~~2,~~ 1, wherein the insulating metal oxide film is an anodic oxide film formed by oxidizing the side and top surfaces of the X wiring lines by anodic oxidation.

4. (Withdrawn) A method of fabricating an electrical circuit board comprising:

a first step of depositing a conductive metal film layer over an insulating substrate;

a second step of etching the conductive metal film layer to simultaneously form X wiring lines and Y segmented wiring lines in a same plane, the Y segmented wiring lines intersecting with the X wiring lines, being severed by the X wiring lines at the intersections, and being distanced from the X wiring lines;

a third step, after the second step, of oxidizing top and side surfaces of the X wiring lines to cover the top and side surfaces by an insulating metal oxide film; and

a fourth step, after the third step, of depositing a conductive film layer so as to cover at least the intersections, whereby segments of each of the Y segmented wiring lines are electrically connected together, each of the Y

segmented wiring lines being severed by and distanced from the X wiring lines.

5. (Withdrawn) The method of fabricating an electrical circuit board according to claim 4, wherein the third step of oxidizing the X wiring lines is carried out by anodic oxidation.

6. (Withdrawn) A method of fabricating an electrical circuit board comprising:

a first step of sequentially depositing at least a conductive metal film layer and an insulating film layer over an insulating substrate;

a second step of etching layers including the insulating film layer and the conductive metal film layer to simultaneously form X wiring lines and Y segmented wiring lines in a same plane, the Y segmented wiring lines intersecting with the X wiring lines, being severed by the X wiring lines at the intersections, and being distanced from the X wiring lines;

a third step, after the second step, of oxidizing side surfaces of the X wiring lines to cover the side surfaces by an insulating metal oxide film; and

a fourth step, after the third step, of depositing a conductive film layer so as to cover at least the intersections,

whereby segments of each of the Y segmented wiring lines are electrically connected together, each of the Y segmented wiring lines being severed by and distanced from the X wiring lines.

7. (Withdrawn) The method of fabricating an electrical circuit board according to claim 6, wherein the third step of oxidizing the side surfaces of the X wiring lines is carried out by anodic oxidation.

8. (Withdrawn) A bottom-gate TFT array substrate comprising:

gate electrodes formed directly on a substrate or with an undercoat film layer disposed between the gate electrodes and the substrate, side surfaces of the gate electrodes being covered with an insulating film;

a gate insulating film stacked on each of the gate electrodes;

a semiconductor film stacked on the gate insulating film, the semiconductor film having source regions, drain regions, and channel regions between the source regions and the drain regions;

source contact electrodes stacked on the source regions of the semiconductor film;

drain contact electrodes stacked on the drain regions of the semiconductor film;

pixel electrodes connected to the drain regions of the semiconductor film by the drain contact electrodes;

gate wiring lines connected to the gate electrodes, top and side surfaces of the gate wiring lines being covered with an insulating film;

source segmented wiring lines formed in a same plane as the gate wiring lines, each of the source segmented wiring lines intersecting with the gate wiring lines in the same plane and being severed by and distanced from the gate wiring lines at the intersections; and

source wiring line-connecting electrodes for electrically connecting segments of each source segmented wiring line together on the gate wiring lines.

9. (Withdrawn) The bottom-gate TFT array substrate according to claim 8, wherein the pixel electrodes and the source wiring line-connecting electrodes are composed of a same transparent conductive film material.

10. (Withdrawn) The bottom-gate TFT array substrate according to claim 9 wherein:

a source segmented wiring line section pattern has a five-layered structure composed of the source segmented wiring lines, a gate insulating film, a semiconductor film, a contact metal film, and a transparent conductive film, and the source segmented wiring lines are located at the bottom of the five-layered structure;

a gate wiring line section pattern has a five-layered structure composed of the gate wiring lines, a gate insulating film, a semiconductor film, a contact metal film, and a transparent conductive film, and the gate wiring lines are located at the bottom of the five-layered structure; and

the source segmented wiring lines and the gate wiring lines are in the same plane on the substrate.

11. (Withdrawn) The bottom-gate TFT array substrate according to claim 10, wherein the insulating film of at least the side surfaces of the gate wiring lines is composed of an oxide film formed from the conductive metal film.

12. (Withdrawn) The bottom-gate TFT array substrate according to claim 11, wherein the oxide film is an anodic oxide film formed by anodic oxidation.

13. (Withdrawn) The bottom-gate TFT array substrate according to claim 11, wherein the semiconductor film has a two-layered structure composed of an i-type amorphous silicon layer and an n-type amorphous silicon layer.

14. (Withdrawn) The bottom-gate TFT array substrate according to claim 9, wherein in place of the transparent conductive film material, a light reflective conductive film material is used.

15. (Withdrawn) A method of fabricating a bottom-gate TFT array substrate comprising:

(A) sequentially depositing at least a G-S metal film layer, a gate insulating film layer, a semiconductor film layer, and a contact metal film layer over a surface of an insulating substrate, the G-S metal film layer to be formed into gate electrodes, gate wiring lines, and source segmented wiring lines;

(B), after step (A), by photolithography, using a first resist pattern, etching the layers through to the surface of the

insulating substrate to form a gate electrode section pattern, a gate wiring line section pattern, and a source segmented wiring line section pattern, the gate electrode section pattern including gate electrodes and the gate metal film, the gate insulating film, the semiconductor film, and the contact metal film which are sequentially stacked on the gate electrodes, the gate wiring line section pattern including gate wiring lines connected to the gate electrodes and the gate metal film, the gate insulating film, the semiconductor film, and the contact metal film which are sequentially stacked on the gate wiring lines, and the source segmented wiring line section pattern including source segmented wiring lines, which are severed and distanced at the intersections of the source segmented wiring lines and the gate wiring lines, and the gate metal film, the gate insulating film, the semiconductor film, and the contact metal film which are sequentially stacked on the source segmented wiring lines;

(C), after step (B), etching the contact metal film of the gate electrode section pattern through to a surface of the semiconductor film to form on the semiconductor film, and oxidizing side surfaces of the gate electrodes and side

surfaces of the gate wiring lines to form an electrically insulating metal oxide film;

(E), after step (C), depositing a transparent conductive film layer on top of the contact metal film over the entire surface of the substrate so that at least segments of each source segmented wiring line are electrically connected together by the conductive film; and

(F), after step (E), by photolithography, using a second resist pattern, etching the transparent conductive film layer in a predetermined pattern to form pixel electrodes and channel regions exposed by the etching.

16. (Withdrawn) The method of fabricating a bottom-gate TFT array substrate according to claim 15, wherein the oxidation of the side surfaces of the gate wiring lines is carried out by anodic oxidation.

17. (Withdrawn) The method of fabricating a bottom-gate TFT array substrate according to claim 15 wherein:

the semiconductor film layer has a two-layered structure composed of an n-type amorphous silicon layer and an i-type amorphous silicon layer; and

step (F) of etching the contact metal film of the gate electrode section pattern is carried out such that part of the contact metal film and part of the n-type amorphous silicon layer immediately below the contact metal film are etched through to the i-type amorphous silicon layer.

18. (Withdrawn) The method of fabricating a bottom-gate TFT array substrate according to claim 15, wherein in place of the transparent conductive film layer in step (E), a light reflective conductive film layer is deposited.

19. (Withdrawn) A liquid crystal display device comprising;

a bottom-gate TFT array substrate including gate electrodes formed directly on a substrate or with an undercoat film layer disposed between the gate electrodes and the substrate, side surfaces of the gate electrodes being covered with an insulating film; a gate insulating film stacked on the gate electrodes; a semiconductor film stacked on the gate insulating film, the semiconductor film having source regions, drain regions, and channel regions between the source regions and the drain regions; source contact electrodes stacked on the source regions of the semiconductor film; drain contact electrodes stacked on the

drain regions of the semiconductor film; pixel electrodes connected to the drain regions of the semiconductor film by the drain contact electrodes; gate wiring lines connected to the gate electrodes, top and side surfaces of the gate wiring lines being covered with an insulating film; source segmented wiring lines formed in a same plane as the gate wiring lines, the source segmented wiring lines intersecting with the gate wiring lines in the same plane and being severed by and distanced from the gate wiring lines at the intersections; and source wiring line-connecting electrodes for electrically connecting segments of each source segmented wiring line together on the gate wiring lines; and

a counter substrate;

wherein the TFT array substrate and the counter substrate are opposed to each other with a surface on which the TFTs are being formed facing inside and with a predetermined gap therebetween, a liquid crystal being held in the gap.

20. (Withdrawn) The liquid crystal display device according to claim 19, wherein a surface of the TFT array substrate is protected by a passivation film.

21. (Withdrawn) The liquid crystal display device according to claim 20, wherein the passivation film is one selected from the group consisting of a silica film and a silicon nitride film.

22. (Withdrawn) The liquid crystal display device according to claim 19, wherein the pixel electrodes are composed of a transparent metal film.

23. (Withdrawn) The liquid crystal display device according to claim 19, wherein the pixel electrodes are composed of a light reflective metal film.

24. (Withdrawn) A bottom-gate TFT array substrate comprising source segmented wiring lines, gate wiring lines, a gate insulating film, a semiconductor film, and a reflective pixel metal electrode group, the bottom-gate TFT array substrate wherein:

at least side surfaces of gate electrodes and side surfaces of the gate wiring lines are oxidized;

each of the reflective pixel metal electrodes has a two-layered structure composed of a contact metal electrode and another metal electrode film and is connected to a drain region of a corresponding TFT by the contact metal electrode; and

each of the source segmented wiring lines is connected to a source region of a corresponding TFT by two layers of a contact metal electrode and a metal electrode.

25. (Withdrawn) The bottom-gate TFT array substrate according to claim 24, wherein the reflective pixel metal electrode group is one selected from the group consisting of aluminum and an aluminum-based alloy.

26. (Withdrawn) The bottom-gate TFT array substrate according to claim 24, wherein part of each source segmented wiring line has a two-layered structure composed of a contact electrode metal film and an aluminum-based metal electrode film.

27. (Withdrawn) The bottom-gate TFT array substrate according to claim 24, wherein the gate insulating film and the semiconductor film are formed between the gate electrode metal and the contact metal electrode.

28. (Withdrawn) The bottom-gate TFT array substrate according to claim 24, wherein the source segmented wiring lines are severed by the gate wiring lines, and segments of each source segmented wiring line are interconnected together on the gate wiring lines

by the two layers of the contact metal electrode and the metal electrode.

29. (Withdrawn) The bottom-gate TFT array substrate according to claim 24, wherein part of the semiconductor film has a two-layered structure composed of an i-type layer and an n+-type layer.

30. (Withdrawn) The bottom-gate TFT array substrate according to claim 24, wherein an undercoat film is formed between a surface of the insulating substrate and the gate wiring line metal film.

31. (Withdrawn) A method of fabricating a bottom-gate TFT array substrate comprising:

forming at least a gate wiring line metal film, a gate insulating film, and a semiconductor film on a surface of an insulating substrate;

by photolithography, sequentially etching the semiconductor film, the gate insulating film, and the gate wiring line metal film, using a first pattern;

oxidizing side surfaces of portions of a gate wiring line metal film pattern to be formed into gate wiring lines and gate electrodes;

forming a contact electrode metal film and a metal electrode film; and

by photolithography, etching part of the metal electrode film, the contact electrode metal film, and the semiconductor film, using a second pattern.

32. (Withdrawn) The method of fabricating a bottom-gate TFT array substrate according to claim 31, wherein the metal electrode film is an aluminum or aluminum-based alloy film.

33. (Withdrawn) The method of fabricating a bottom-gate TFT array substrate according to claim 31, further comprising forming a silica-based undercoat film between the surface of the insulating substrate and the gate wiring line metal film.

34. (Withdrawn) The method of fabricating a bottom-gate TFT array substrate according to claim 31, wherein at least an aluminum-based alloy film is formed for the gate wiring line metal film.

35. (Withdrawn) The method of fabricating a bottom-gate TFT array substrate according to claim 31, wherein the oxidation is carried out, by anodic oxidation, in a neutral solution.

36. (Withdrawn) A liquid crystal display device comprising:

a bottom-gate TFT array substrate having an array side, the array side including gate electrodes and gate wiring lines, at least side surfaces of the gate electrodes and side surfaces of the gate wiring lines being oxidized; reflective pixel metal electrodes each having a two-layered structure composed of a contact metal electrode and another metal electrode film and being connected to a drain region of a corresponding TFT by the contact metal electrode; and source segmented wiring lines each connected to a source region of a corresponding TFT by two layers of a contact metal electrode and a metal electrode; and

a color filter substrate having a color filter side on which a counter transparent electrode is formed;

wherein the bottom-gate TFT array substrate and the color filter substrate are adhered together with the array side and the color filter side opposing to each other and with a predetermined gap maintained between the substrates, a liquid crystal being sandwiched in the gap and an alignment film being disposed on each of the substrates.

37. (Withdrawn) The liquid crystal display device according to claim 36, wherein at least part of the TFT array is covered with a passivation film.

38. (Withdrawn) The liquid crystal display device according to claim 37, wherein the passivation film is an inorganic substance.

39. (Withdrawn) A method of fabricating a liquid crystal display device comprising:

fabricating a bottom-gate TFT array substrate including forming at least a gate wiring line metal film, a gate insulating film, and a semiconductor film on a surface of an insulating substrate; by photolithography, sequentially etching the semiconductor film, the gate insulating film, and the gate wiring line metal film, using a first pattern; oxidizing side surfaces of portions of a gate wiring line metal film pattern to be formed into gate wiring lines and gate electrodes; forming a contact electrode metal film and a metal electrode film; and by photolithography, etching part of the metal electrode film, the contact electrode metal film, and the semiconductor film, using a second pattern;

forming an alignment film on the bottom-gate TFT array substrate;

forming an alignment film on a surface of a counter electrode side of a color filter substrate having a counter transparent electrode formed thereon;

adhering and fixing the bottom-gate TFT array substrate and the color filter substrate at the periphery thereof such that the substrates are arranged with the two alignment films facing inside and with a predetermined gap maintained between the substrates; and

injecting a specified liquid crystal between the first and second substrates.

40. (Withdrawn) The method of fabricating a liquid crystal display device according to claim 39, further comprising, after the fabrication of the bottom-gate TFT array substrate prior to the formation of the alignment films, covering at least part of the TFT array by a passivation film.

41. (Withdrawn) The method of fabricating a liquid crystal display device according to claim 39, wherein the metal electrode and the contact metal electrode are formed in a single layer with a same material.

42. (Withdrawn) A bottom-gate TFT array substrate comprising source segmented wiring lines, gate wiring lines, a gate insulating film, a semiconductor film, and a comb-shaped pixel metal electrode group, the bottom-gate TFT array substrate wherein:

at least side surfaces of gate electrodes, side surfaces of the gate wiring lines, and side surfaces of the first comb-shaped pixel electrodes are oxidized;

each of the second comb-shaped pixel metal electrodes is connected to a drain region of a corresponding TFT by a contact electrode metal; and

each of the source segmented wiring lines is connected to a source region of a corresponding TFT by a contact electrode metal and a metal electrode.

43. (Withdrawn) The bottom-gate TFT array substrate according to claim 42, wherein the oxide film of the side surfaces of the gate electrodes and of the first comb-shaped pixel electrodes is an anodic oxide film.

44. (Withdrawn) The bottom-gate TFT array substrate according to claim 42, wherein the first comb-shaped pixel electrodes and part of each source segmented wiring line have a five-layered

structure composed of a gate wiring line metal film, a semiconductor film, a contact electrode metal film, and a metal electrode film.

45. (Withdrawn) The bottom-gate TFT array substrate according to claim 42, wherein the contact electrode metal is formed to connect each of the comb-shaped electrodes to the semiconductor film.

46. (Withdrawn) The bottom-gate TFT array substrate according to claim 42, wherein the source segmented wiring lines are severed by the gate wiring lines and the first comb-shaped electrodes, and segments of each source segmented wiring line are interconnected together on the gate wiring lines and the first comb-shaped electrodes by a contact electrode metal and the metal electrode.

47. (Withdrawn) The bottom-gate TFT array substrate according to claim 42, wherein part of the semiconductor film has a two-layered structure composed of an i-type layer and an n-type layer.

48. (Withdrawn) The bottom-gate TFT array substrate according to claim 42, wherein an undercoat film is formed between a surface of the insulating substrate and a gate wiring line metal film.

49. (Withdrawn) A method of fabricating a bottom-gate TFT array substrate comprising:

forming at least a gate wiring line metal film, a gate insulating film, a semiconductor film, and a contact electrode metal film on a surface of an insulating substrate;

by photolithography, sequentially etching the contact electrode metal film, the semiconductor film, the gate insulating film, and the gate wiring line metal film, using a first pattern;

oxidizing side surfaces of portions of a metal film pattern to be formed into gate wiring lines, gate electrodes, and first comb-shaped pixel electrodes;

forming a metal electrode film; and

by photolithography, sequentially etching part of the metal electrode film, the contact electrode metal film, and the semiconductor film, using a second pattern.

50. (Withdrawn) The method of fabricating a bottom-gate TFT array substrate according to claim 49, wherein portions to be formed into the gate wiring lines, the gate electrodes, and the first comb-shaped pixel electrodes are simultaneously etched.

51. (Withdrawn) The method of fabricating a bottom-gate TFT array substrate according to claim 49, further comprising forming an undercoat film between the surface of the insulating substrate and the gate wiring line metal film.

52. (Withdrawn) The method of fabricating a bottom-gate TFT array substrate according to claim 49, wherein at least the gate wiring line metal film, the gate insulating film, and the semiconductor film are sequentially formed.

53. (Withdrawn) The method of fabricating a bottom-gate TFT array substrate according to claim 49, wherein the oxidation is carried out by anodic oxidation.

54. (Withdrawn) A liquid crystal display device comprising:

a bottom-gate TFT array substrate having an electrode side, the electrode side including gate electrodes, gate wiring

lines, and first comb-shaped electrodes, at least side surfaces of the gate electrodes, of the gate wiring lines, and of the first comb-shaped electrodes being oxidized; second comb-shaped pixel metal electrodes each connected to a drain region of a corresponding TFT by a contact electrode metal; and source segmented wiring lines each connected to a source region of a corresponding TFT by a contact electrode metal and a metal electrode; and

a color filter substrate having a color filter side;

wherein the bottom-gate TFT array substrate and the color filter substrate are adhered together with the electrode side and the color filter side opposing to each other and with a predetermined gap maintained between the substrates, a liquid crystal being sandwiched in the gap and an alignment film being disposed on each of the substrates.

55. (Withdrawn) The liquid crystal display device according to claim 54, wherein at least part of the TFT array is covered with a passivation film.

56. (Withdrawn) The liquid crystal display device according to claim 55, wherein the passivation film is an inorganic substance.

57. (Withdrawn) A method of fabricating a liquid crystal display device comprising:

fabricating a bottom-gate TFT array substrate including forming at least a gate wiring line metal film, a gate insulating film, a semiconductor film, and a contact electrode metal film on a surface of an insulating substrate; by photolithography, sequentially etching the contact electrode metal film, the semiconductor film, the gate insulating film, and the gate wiring line metal film, using a first pattern; oxidizing side surfaces of portions of a metal film pattern to be formed into gate wiring lines, gate electrodes, and first comb-shaped pixel electrodes; forming a metal electrode film; and by photolithography, sequentially etching part of the metal electrode film, the contact electrode metal film, and the semiconductor film, using a second pattern;

forming an alignment film on the bottom-gate TFT array substrate;

forming an alignment film on a surface of a color filter substrate;

adhering and fixing the bottom-gate TFT array substrate and the color filter substrate at the periphery thereof such that the substrates are arranged with the two alignment films

facing inside and with a predetermined gap maintained between the substrates; and

injecting a specified liquid crystal between the first and second substrates.

58. (Withdrawn) The method of fabricating a liquid crystal display device according to claim 57, further comprising:

after the fabrication of the bottom-gate TFT array substrate prior to the formation of the alignment films, covering at least part of the TFT array by a passivation film; and

using the passivation film as a mask, etching the metal electrode film, the contact electrode metal film, the semiconductor film, and the gate insulating film, to expose gate wiring line terminals.

59. (Withdrawn) The method of fabricating a liquid crystal display device according to claim 58, wherein the passivation film is a silica film or a silicon nitride film.

60. (Withdrawn) A bottom-gate TFT array substrate comprising source segmented wiring lines, gate wiring lines, a gate insulating film, a semiconductor film, and a comb-shaped pixel

metal electrode group, the bottom-gate TFT array substrate wherein:

at least side surfaces of gate electrodes and side surfaces of the gate wiring lines are oxidized;

each of the comb-shaped reflective pixel metal electrodes has a two-layered structure composed of a contact metal electrode and another metal electrode film and is connected to a drain region of a corresponding TFT by the contact metal electrode; and

each of the source segmented wiring lines is connected to a source region of a corresponding TFT by two layers of a contact metal electrode and a metal electrode.

61. (Withdrawn) The bottom-gate TFT array substrate according to claim 60, wherein an aluminum-based metal is used for the gate electrodes, and the insulating film of the side surfaces is an anodic oxide film.

62. (Withdrawn) The bottom-gate TFT array substrate according to claim 60, wherein part of each source segmented wiring line has a five-layered structure composed of a gate wiring line metal film, a gate insulating film, a semiconductor film, a contact electrode metal film, and a metal electrode film.

63. (Withdrawn) The bottom-gate TFT array substrate according to claim 60, wherein the contact metal electrode is formed between a source electrode and the semiconductor film and between the comb-shaped electrode and the semiconductor film.

64. (Withdrawn) The bottom-gate TFT array substrate according to claim 60, wherein the source segmented wiring lines are severed by the gate wiring lines, and segments of each source segmented wiring line are interconnected together on the gate wiring lines by the two layers of the contact metal electrode and the metal electrode.

65. (Withdrawn) The bottom-gate TFT array substrate according to claim 60, wherein part of the semiconductor film has a two-layered structure composed of an i-type layer and an n-type layer.

66. (Withdrawn) The bottom-gate TFT array substrate according to claim 60, wherein an undercoat film is formed between a surface of the insulating substrate and the gate wiring line metal film.

67. (Withdrawn) A method of fabricating a bottom-gate TFT array substrate comprising:

forming at least a gate wiring line metal film, a gate insulating film, and a semiconductor film on a surface of an insulating substrate;

by photolithography, sequentially etching the semiconductor film, the gate insulating film, and the gate wiring line metal film, using a first pattern;

oxidizing side surfaces of portions of a gate wiring line metal film pattern to be formed into gate wiring lines, gate electrodes, and first comb-shaped electrodes;

forming a contact electrode metal film and a metal electrode film; and

by photolithography, etching part of the metal electrode film, the contact electrode metal film, and the semiconductor film, using a second pattern.

68. (Withdrawn) The method of fabricating a bottom-gate TFT array substrate according to claim 67, wherein the semiconductor film has a two-layered structure composed of an i-type layer and an n-type layer, and part of the n-type layer is etched through to the i-type layer.

69. (Withdrawn) The method of fabricating a bottom-gate TFT array substrate according to claim 67, further comprising forming an undercoat film between the surface of the insulating substrate and the gate wiring line metal film.

70. (Withdrawn) The method of fabricating a bottom-gate TFT array substrate according to claim 67, wherein at least the gate wiring line metal film, the gate insulating film, and the semiconductor film are sequentially formed.

71. (Withdrawn) The method of fabricating a bottom-gate TFT array substrate according to claim 67, wherein the oxidation is carried out by anodic oxidation.

72. (Withdrawn) A liquid crystal display device comprising:

a bottom-gate TFT array substrate having an array side, the array side including gate electrodes and gate wiring lines, at least side surfaces of the gate electrodes and side surfaces of the gate wiring lines being oxidized; first comb-shaped pixel metal electrodes each having a two-layered structure composed of a contact metal electrode and another metal electrode film and being connected to a drain region of a corresponding TFT by the contact metal

electrode; and source segmented wiring lines each connected to a source region of a corresponding TFT by two layers of a contact metal electrode and a metal electrode; and

a color filter substrate having a color filter side;

wherein the bottom-gate TFT array substrate and the color filter substrate are adhered together with the array side and the color filter side opposing to each other and with a predetermined gap maintained between the substrates, a liquid crystal being sandwiched in the gap and an alignment film being disposed on each of the substrates.

73. (Withdrawn) The liquid crystal display device according to claim 72, wherein at least part of the TFT array is covered with a passivation film.

74. (Withdrawn) The liquid crystal display device according to claim 72, wherein the passivation film is an inorganic substance.

75. (Withdrawn) A method of fabricating a liquid crystal display device comprising:

fabricating a bottom-gate TFT array substrate including forming at least a gate wiring line metal film, a gate insulating film, and a semiconductor film on a surface of an

insulating substrate; by photolithography, sequentially etching the semiconductor film, the gate insulating film, and the gate wiring line metal film, using a first pattern; oxidizing side surfaces of portions of a gate wiring line metal film pattern to be formed into gate wiring lines, gate electrodes, and first comb-shaped electrodes; forming a contact electrode metal film and a metal electrode film; by photolithography, etching part of the metal electrode film, the contact electrode metal film, and the semiconductor film, using a second pattern;

forming an alignment film on the bottom-gate TFT array substrate;

forming an alignment film on a surface of a counter electrode side of a color filter substrate;

adhering and fixing the bottom-gate TFT array substrate and the color filter substrate at the periphery thereof such that the substrates are arranged with the two alignment films facing inside and with a predetermined gap maintained between the substrates; and

injecting a specified liquid crystal between the first and second substrates.

76. (Withdrawn) The method of fabricating a liquid crystal display device according to claim 75, further comprising, after the fabrication of the bottom-gate TFT array substrate prior to the formation of the alignment films, covering at least part of the TFT array by a passivation film.

77. (Withdrawn) The method of fabricating a liquid crystal display device according to claim 75, wherein the metal electrode and the contact metal electrode are formed in a single layer with a same material.

78. (Withdrawn) A bottom-gate TFT array substrate comprising source segmented wiring lines, gate wiring lines, a gate insulating film, a semiconductor film, and a comb-shaped pixel electrode group, the bottom-gate TFT array substrate wherein:

at least side surfaces of gate electrodes and side surfaces of the gate wiring lines are oxidized;

each of the first comb-shaped pixel electrodes is connected to a drain region of a corresponding TFT by a contact electrode metal;

each of the source segmented wiring lines is connected to a source region of a corresponding TFT by a contact electrode metal and a metal electrode; and

the second comb-shaped opposing electrodes are formed with an insulating film disposed between the second comb-shaped opposing electrodes and the substrate.

79. (Withdrawn) The bottom-gate TFT array substrate according to claim 78, wherein the oxide film of the side surfaces of the gate electrodes is an anodic oxide film.

80. (Withdrawn) The bottom-gate TFT array substrate according to claim 78, wherein part of each source segmented wiring line has a five-layered structure composed of a gate wiring line metal film, a semiconductor film, a contact electrode metal film, and a metal electrode film.

81. (Withdrawn) The bottom-gate TFT array substrate according to claim 78, wherein the contact electrode metal is formed between the semiconductor film and a source electrode and between the semiconductor film and a drain electrode.

82. (Withdrawn) The bottom-gate TFT array substrate according to claim 78, wherein the source segmented wiring lines are severed by the gate wiring lines, and segments of each source segmented wiring line are interconnected together on the gate wiring lines by a contact electrode metal and the metal electrode.

83. (Withdrawn) The bottom-gate TFT array substrate according to claim 78, wherein part of the semiconductor film has a two-layered structure composed of an i-type layer and an n-type layer.

84. (Withdrawn) The bottom-gate TFT array substrate according to claim 78, wherein an undercoat film is formed between a surface of the insulating substrate and the gate wiring line metal film.

85. (Withdrawn) A method of fabricating a bottom-gate TFT array substrate comprising:

forming at least a gate wiring line metal film, a gate insulating film, a semiconductor film, and a contact electrode metal film on a surface of an insulating substrate;

by photolithography, sequentially etching the contact electrode metal film, the semiconductor film, the gate insulating

film, and the gate wiring line metal film, using a first pattern;

oxidizing side surfaces of portions of a metal film pattern to be formed into gate wiring lines and gate electrodes;

forming a metal electrode film;

by photolithography, sequentially etching part of the metal electrode film, the contact electrode metal film, and the semiconductor film, using a second pattern; and

forming second comb-shaped opposing electrodes using a third pattern with an insulating film disposed between the second comb-shaped opposing electrodes and the substrate.

86. (Withdrawn) The method of fabricating a bottom-gate TFT array substrate according to claim 85, wherein the semiconductor film has a two-layered structure composed of an i-type layer and an n-type layer, and part of the n-type layer is etched.

87. (Withdrawn) The method of fabricating a bottom-gate TFT array substrate according to claim 85, further comprising forming an undercoat film between the surface of the insulating substrate and the gate wiring line metal film.

88. (Withdrawn) The method of fabricating a bottom-gate TFT array substrate according to claim 85, wherein at least the gate wiring line metal film, the gate insulating film, and the semiconductor film are sequentially formed.

89. (Withdrawn) The method of fabricating a bottom-gate TFT array substrate according to claim 85, wherein the oxidation is carried out by anodic oxidation.

90. (Withdrawn) A liquid crystal display device comprising:

a bottom-gate TFT array substrate having an electrode side, the electrode side including gate electrodes and gate wiring lines, at least side surfaces of the gate electrodes and side surfaces of the gate wiring lines being oxidized; first comb-shaped pixel metal electrodes each connected to a drain region of a corresponding TFT by a contact electrode metal; source segmented wiring lines each connected to a source region of a corresponding TFT by a contact electrode metal and a metal electrode; and second comb-shaped opposing electrodes formed with an insulating film disposed between the second comb-shaped opposing electrodes and the substrate; and

a color filter substrate having a color filter side;

wherein the bottom-gate TFT array substrate and the color filter substrate are adhered together with the electrode side and the color filter side opposing to each other and with a predetermined gap maintained between the substrates, a liquid crystal being sandwiched in the gap and an alignment film being disposed on each of the substrates.

91. (Withdrawn) The liquid crystal display device according to claim 90, wherein at least part of the TFT array is covered with a passivation film.

92. (Withdrawn) The liquid crystal display device according to claim 91, wherein the passivation film is an inorganic substance.

93. (Withdrawn) A method of fabricating a liquid crystal display device comprising:

fabricating a bottom-gate TFT array substrate including forming at least a gate wiring line metal film, a gate insulating film, a semiconductor film, and a contact electrode metal film on a surface of an insulating substrate; by photolithography, sequentially etching the contact electrode metal film, the semiconductor film, the gate insulating film, and the gate wiring line metal film, using

a first pattern; oxidizing side surfaces of portions of a metal film pattern to be formed into gate wiring lines and gate electrodes; forming a metal electrode film; by photolithography, sequentially etching part of the metal electrode film, the contact electrode metal film, and the semiconductor film, using a second pattern; and forming second comb-shaped opposing electrodes, using a third pattern, with a passivation film disposed between the second comb-shaped opposing electrodes and the substrate;

forming an alignment film on the bottom-gate TFT array substrate;

forming an alignment film on a surface of a color filter side of a color filter substrate;

adhering and fixing the bottom-gate TFT array substrate and the color filter substrate at the periphery thereof such that the substrates are arranged with the two alignment films facing inside and with a predetermined gap maintained between the substrates; and

injecting a specified liquid crystal between the first and second substrates.

94. (Withdrawn) The method of fabricating a liquid crystal display device according to claim 93, further comprising, after the formation of the second comb-shaped opposing electrodes, covering at least part of each second comb-shaped opposing electrode by a passivation film.

95. (Withdrawn) The method of fabricating a liquid crystal display device according to claim 93, wherein the passivation film is a silica film or a silicon nitride film.

96. (Withdrawn) A bottom-gate TFT array substrate comprising source segmented wiring lines, gate wiring lines, a gate insulating film, a semiconductor film, and a comb-shaped pixel electrode group, the bottom-gate TFT array substrate wherein:

at least side surfaces of gate electrodes and side surfaces of the gate wiring lines are oxidized;

each of the first comb-shaped pixel metal electrodes has a two-layered structure composed of a contact electrode metal and is connected to a drain region of a corresponding TFT;

each of the source segmented wiring lines is connected to a source region of a corresponding TFT by a contact electrode metal and a metal electrode; and

the second comb-shaped opposing electrodes are formed with an insulating film disposed between the second-comb shaped opposing electrodes and the substrate.

97. (Withdrawn) The bottom-gate TFT array substrate according to claim 96, wherein at least segments of each source segmented wiring line are connected together by a two-layered structure composed of the metal electrode and a contact electrode metal.

98. (Withdrawn) A method of fabricating a bottom-gate TFT array substrate comprising:

forming at least a gate wiring line metal film, a gate insulating film, and a semiconductor film on a surface of an insulating substrate;

by photolithography, sequentially etching the semiconductor film, the gate insulating film, and the gate wiring line metal film, using a first pattern;

oxidizing side surfaces of portions of a metal film pattern to be formed into gate wiring lines and gate electrodes;

forming a contact electrode metal film and a metal electrode film;

by photolithography, sequentially etching part of the metal electrode film, the contact electrode metal film, and the semiconductor film, using a second pattern; and

forming second comb-shaped opposing electrodes, using a third pattern, with an insulating film disposed between the second comb-shaped opposing electrodes and the substrate.

99. (Withdrawn) A liquid crystal display device comprising:

a bottom-gate TFT array substrate having an electrode side, the electrode side including gate electrodes and gate wiring lines, at least side surfaces of the gate electrodes and side surfaces of the gate wiring lines being oxidized; first comb-shaped pixel electrodes each having a two-layered structure composed of a contact electrode metal and being connected to a drain region of a corresponding TFT; source segmented wiring lines each connected to a source region of a corresponding TFT by a contact electrode metal and a metal electrode; and second comb-shaped opposing electrodes formed with an insulating film disposed between the second comb-shaped opposing electrodes and the substrate; and

a color filter substrate having a color filter side;

wherein the bottom-gate TFT array substrate and the color filter substrate are adhered together with the electrode side and the color filter side opposing to each other and with a predetermined gap maintained between the substrates, a liquid crystal being sandwiched in the gap and an alignment film being disposed on each of the substrates.

100. (Withdrawn) A method of fabricating a liquid crystal display device comprising:

fabricating a bottom-gate TFT array substrate including forming at least a gate wiring line metal film, a gate insulating film, and a semiconductor film on a surface of an insulating substrate; by photolithography, sequentially etching the semiconductor film, the gate insulating film, and the gate wiring line metal film, using a first pattern; oxidizing side surfaces of portions of a metal film pattern to be formed into gate wiring lines and gate electrodes; forming a contact electrode metal film and a metal electrode film; by photolithography, sequentially etching part of the metal electrode film, the contact electrode metal film, and the semiconductor film, using a second pattern; and forming second comb-shaped opposing

electrodes, using a third pattern, with an insulating film disposed between the second comb-shaped opposing electrodes and the substrate;

forming an alignment film on the bottom-gate TFT array substrate;

forming an alignment film on a surface of a color filter side of a color filter substrate;

adhering and fixing the bottom-gate TFT array substrate and the color filter substrate at the periphery thereof such that the substrates are arranged with the two alignment films facing inside and with a predetermined gap maintained between the substrates; and

injecting a specified liquid crystal between the first and second substrates.

101. (Withdrawn) The method of fabricating a liquid crystal display device according to claim 100, further comprising covering at least part of each second comb-shaped opposing electrode by a passivation film.

102. (New) An electrical circuit board comprising:

X wiring lines and Y segmented wiring lines, each of the wiring lines comprising a same conductive metal film and in a same plane on an insulating substrate and the Y segmented wiring lines intersecting the X wiring lines and being severed at the intersections with the X wiring lines and spaced apart from the X wiring lines;

wherein top and side surfaces of the X wiring lines are covered with an insulating film of an oxide of said same conductive metal;

wherein segments of each of the Y segmented wiring lines are electrically connected together by a Y segmented wiring line-connecting electrode formed on the insulating film, the segments being spaced apart by the X wiring lines and the covering insulating metal oxide film.

103. (New) The electrical circuit board according to claim 102, wherein the insulating metal oxide film is an anodic oxide film on the top and side surfaces of the X wiring lines.